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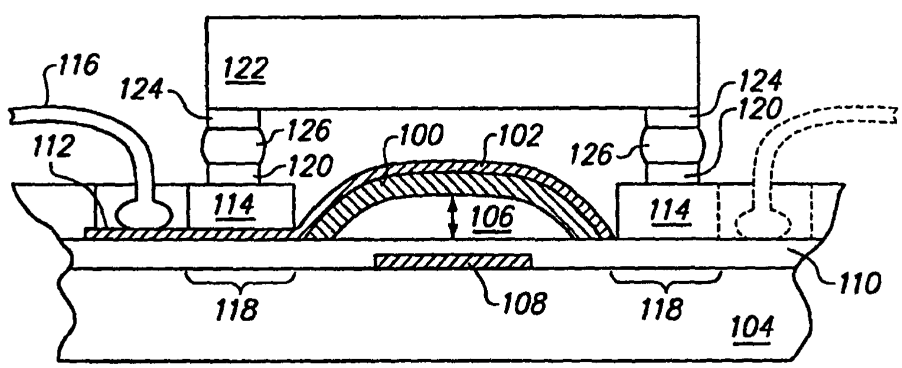

(57) Abstract

A method and apparatus of hermetically passivating a semiconductor device includes sealing a lid directly onto a semiconductor substrate. An active device is formed on the surface of the substrate and is surrounded by a substantially planar lid sealing region, which in turn is surrounded by bonding pads. A first layer of solderable material is formed on the lid sealing region. A lid is provided which has a second layer of solderable material in a configuration corresponding to the first layer. A solder is provided between the first layer and second layer of solderable materials. In the preferred embodiment, the solder is formed over the second layer. Heat is provided to hermetically join the lid to the semiconductor device without requiring a conventional package. Preferably the first and second layers are sandwiches of conventionally known solderable materials which can be processed using conventional semiconductor techniques. An angle between the lid and the semiconductor device can be controlled by adjusting relative widths of one or both the layers of solderable materials.

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METHOD OF AND APPARATUS FOR SEALING AN HERMETIC LID TO A SEMICONDUCTOR DIE

Field of the Invention

This invention relates to the field of passivating semiconductor die, especially hermetically. More particularly, this invention relates to mounting and sealing an optically transparent lid onto an optically active semiconductor integrated circuit.

Background of the Invention

In the manufacture of integrated circuits (chips) it is well known that it is desirable to encapsulate the chip protected from mechanical damage and contamination. These techniques are known to passivate the chips. There are a variety of well known techniques available for encapsulating the chip. These techniques include mounting the chip within a cavity in a package, wire bonding the chip to a lead frame and then enclosing the package with a lid. Another well known technique includes mounting the chip to a lead frame, wire bonding the chip to the lead frame and then passivating the chip and a portion of the lead frame in a molded plastic or plastic epoxy body. A third common technique for passivating a chip includes flip-chip bonding the chip to a printed circuit board and then covering the chip with a plastic resin.

An EPROM is a read-only memory device. The program or data which is stored in an EPROM can only be erased by causing or allowing optical radiation (ultraviolet and visible) to impinge on the surface of the EPROM. Accordingly, conventional chip packaging techniques are inadequate because they are opaque to optical radiation. To solve this problem, makers of EPROMs mount the EPROM chip within the cavity of a ceramic package and hermetically seal the assembly with an optically transparently lid.

Micro-electro-mechanical devices (MEMs) are another well known class of silicon

semiconductors devices. MEMs are useful for a variety of applications including strain gauges, accelerometers, electronic levels, and also for displays or other optical devices. Because of their extremely small moving parts, MEMs are particularly susceptible to ambient conditions. Accordingly, MEMs are traditionally sealed within the cavity of an hermetic package which is then hermetically sealed to control the environment to which the MEM is subjected.

When the MEM is to be used in a display application, it is required that optical energy (light) be able to penetrate the package, impinge on the surface of the MEM for modulation, and then escape from the package for forming a display image. The ability of light to enter and leave the package is also required for other optical devices as well. Though conventional ceramic packages are hermetic, because they are opaque they are unsuitable for use with a display or optical MEM. In certain display or optical MEM applications, the MEM is mounted within the cavity of a ceramic package. The assembly is made hermetic by affixing a transparent lid to the ceramic package with an hermetic seal in much the same way as an EPROM package.

It is well known that much of the cost associated with manufacturing silicon semiconductor devices is incurred through the packaging technology. This is particularly true with hermetic ceramic packages. The cost of packages including an optically transparent window is considerably more expensive still.

Under certain circumstances when building a display or other optical MEM assembly it is important that the MEM and transparent lid have a precise physical relationship to one another. For some applications, it is important that the MEM and transparent lid be precisely parallel to one another. For other applications, it is important

that the MEM and transparent lid are a precise angle between the structures. Conventional silicon semiconductor chip packaging technology does not take into account an ability to control an angle between the chip and the package lid.

What is needed is a method of and an apparatus for hermetically sealing MEMs intended for use in a display application. What is needed is a method of and an apparatus for hermetically sealing MEMs intended for use in an optical application. What is further needed is a method of and an apparatus for sealing MEMs having a high pin count. Also what is needed is a method of and an apparatus for protecting MEMs which is relatively inexpensive. There is a need for a method of and an apparatus for hermetically sealing the display MEM which can be mounted to the MEM through an uncomplicated manufacturing process. What is further needed is a method and apparatus for sealing display MEMs where an angle of the lid relative to the MEM can be precisely controlled through the assembly process.

Summary of the Invention

A method and apparatus of hermetically passivating a semiconductor device includes sealing a lid directly onto a semiconductor substrate. An active device is formed on the surface of the substrate and is surrounded by a substantially planar lid sealing region, which in turn is surrounded by bonding pads. A first layer of solderable material is formed on the lid sealing region. A lid is provided which has a second layer of solderable material in a configuration corresponding to the first layer. A solder layer is provided between the first layer and second layer of solderable materials. In the preferred embodiment, the solder is formed over the second layer. Heat is provided to hermetically join the lid to the semiconductor device without requiring a conventional package. Preferably the first and second layers are sandwiches of conventionally known solderable materials which can be processed using conventional semiconductor techniques. An angle between the lid and the semiconductor device can be controlled by adjusting relative widths of one or both the layers of solderable materials.

Alternatively, the lid can be sealed to the substrate using other techniques. In a first alternative, an epoxy can be used. An optional first spacing material is formed in the lid sealing region. An epoxy is formed in a configuration corresponding to the lid sealing region. The lid and the semiconductor device are aligned and heated to hermetically join them together.

In a second alternative, a glass frit can be used. An optional second spacing material is formed in the lid sealing region. A glass frit is formed in a configuration corresponding to the lid sealing region. The lid and the semiconductor device are aligned and heated to hermetically join them together.

Brief Description of the Drawings

Figure 1 shows a simplified cross section view of the preferred embodiment.

Figure 2 shows a block diagram exemplary plan view of semiconductor device according to the present invention.

Figure 3 shows a simplified schematic cross section diagram of the lid and the semiconductor device prior to sealing the lid.

Figure 4 shows a simplified schematic cross section diagram of the lid sealed to the semiconductor device according to the present invention with somewhat more detail than Figure 3.

Figure 5 shows a schematic cross section diagram of the lid according to the present invention with somewhat more detail than Figure 3 .

Figure 6 shows a schematic cross section diagram of an alternate embodiment of the lid according to the present invention with somewhat more detail than Figure 3.

Figure 7 shows a schematic cross section diagram of the semiconductor device lid according to the present invention with somewhat more detail than Figure 3 .

Figure 8 shows a schematic cross section diagram of an alternate embodiment of the semiconductor device according to the present invention with somewhat more detail than Figure 3.

Figure 9 shows a schematic cross section of an embodiment for generating a predetermined angle of tilt prior to sealing the lid to the semiconductor device.

Figure 10 shows an exaggerated schematic cross section of the embodiment of Figure 9 tilted in place after the lid is sealed to the semiconductor device.

Figure 11 shows a plan view of a fixture for aligning the lid to the semiconductor

device.

Figure 12 shows a side view of the fixture of Figure 11.

Figure 13 shows a graph representing temperature versus time for a process of sealing a lid to a semiconductor device according to the present invention.

Figure 14 shows a graph representing pressure versus time for the process of sealing a lid to a semiconductor device according to the present invention.

Figure 15 shows a schematic cross sectional representation of a wafer saw concurrently separating lids and semiconductor devices.

Detailed Description of the Preferred Embodiment

The present invention was developed to hermetically seal the mechanically active portion of a MEM for display device. In particular, the MEM is a diffraction grating light valve (GLV). Examples of the GLV are found U.S. patent No. 5,311,360 and also in allowed U.S. patent application No. 08/482,188. The developers of this technology have learned that if ambient moisture becomes deposited upon the ribbon structures that surface charging occurs which prevents suitable operation of the GLV. To avoid this sort of problem, it is preferable that the mechanically active portion of the MEM structure is passivated in an hermetic package. In addition, it is important that seal the form of glass or other transparent material having suitable optical characteristics.

In contrast to other prior art hermetically passivating technologies for a silicon semiconductor device, the hermetic lid of the present invention is sealed directly onto the surface of the silicon semiconductor device. It will be readily apparent to those ordinary skill in the art that the passivating technology of the present invention can also be used for

hermetically sealing other types of devices including non-silicon or non-semiconductor devices or for use with non-transparent lid structures.

Figure 1 shows a representative cross section view of the silicon semiconductor device to which the transparent lid is hermetically sealed. The silicon semiconductor device of preferred embodiment is a GLV for forming a display. The cross-section drawing Figure 1 is not drawn to scale nor does it include all the elements necessarily found in an operational GLV. These omissions are not intended to be limiting but rather are made in this document to avoid obscuring the invention in unnecessary and extraneous details.

A conductive ribbon 100 including a metallic conductive and reflective covering 102 is formed over the semiconductor substrate 104 with an air gap 106 between the ribbon 100 and the substrate 104. A conductive electrode 108 is formed on the surface of the substrate 104 and is covered by an insulating layer 110. The conductive electrode 108 is positioned underneath the ribbon 100 and also will be below the air gap 104. The reflective covering 102 extends beyond the region of the mechanically active ribbon 100 and is configured as a conventional bond pad 112 and its distal end. The device is passivated with a conventional overlying insulating passivation layer 114. The passivation layer 114 does not cover the bond pads 112 nor the ribbon structures 100/102. Control and power signals are coupled to the semiconductor device using conventional wire bonding structures 116.

According to conventional semiconductor manufacturing techniques, devices are packed as densely onto the surface of the semiconductor substrate as possible. Here however, because the optical glass is hermetically sealed directly onto the semiconductor

device, the bond pads 112 are removed a considerable distance from the ribbon structures 100/102 to provide a lid sealing region 118. Solderable material 120 is formed onto the lid sealing regions 118 using conventional semiconductor processing techniques.

Because the preferred application for the present invention is for hermetically sealing a GLV for use in a display application, the lid 122 is preferably formed of optical quality material. It will be understood by persons of ordinary skill in the art that the lid 122 can be coated with an optically sensitive material for any of a variety of purposes including but not limited to filtering unwanted radiation, enhancing reflectivity, or decreasing reflectivity. Additionally, the lid 122 can also be configured to have optical characteristics. In other words, the lid 122 can be a lens of any convenient type.

Once the lid is formed to a size appropriate to fit come currently over the lid sealing regions 118 a solderable material 124 is formed in a ring surrounding the periphery of one face of the lid 122 using conventional semiconductor processing techniques. Next, a solder 126 is deposited onto the solderable material 124 so that the lid can be joined to the semiconductor device. Though not shown to scale, it is clear from the drawing of Figure 1 that the lid 122 and the ribbon structures 100/102 are mounted away to avoid interfering with one another. In this way, the written structures 100/102 are free to move upwardly and downwardly.

Figure 2 shows a plan view of an exemplary device according to the present invention wherein the various regions are shown as blocks. It will be apparent to persons ordinary skill in the art that the precise dimensions and ratios between the various structures can be modified to significantly and still fall within the spirit and scope of these teachings. According to the preferred embodiment of the present invention to lid is in

optical element intended for mounting over a GLV to be used as a display engine. The ribbon structures of the GLV comprise a mechanically active region 140. Surrounding the mechanically active region 140 is located the lid sealing region 118. Where appropriate, identical reference numerals will be used in the several drawings to identify the same elements. As previously described, the lid sealing region 118 is passivated and includes no mechanically active elements such as traditionally found in a MEM device. Similarly, the lid sealing region 118 also includes no bond pads were other off chip interface structures as the lid would interfere with the effective operation of such. It is possible that the lid sealing region 118 could include active electronic elements. However, in the event that the lid sealing region 118 did include active electronic elements effort must be taken to planarize that region in order to provide the surface to which the lid can properly mate.

The bonding region 142 surrounds the lid sealing region 118. The bonding region 142 includes the several bond pads necessary for making interconnection from the semiconductor device to off-chip circuits and systems. In the case of the display element such as the GLV of the present invention more than one thousand bond pads are required. Other types of semiconductor devices will require more or fewer bond pads depending upon their intended application.

Figure 3 shows a schematic cross-sectional representation of a first embodiment of present invention. As previously discussed a solderable material 150 is formed onto the lid sealing region 152 of the semiconductor device 154. A solderable material 156 is also formed around the peripheral edges of the transparent lid 158. A layer of solder 160 is formed over the layer of solderable material 156. It will be apparent to one of ordinary skill in the art that the solder could also be applied to the first layer of solderable material.

However, the inventors prefer applying the solder to the lid to avoid contaminating the wafer with solder.

The transparent lid 158 is brought into contact with and aligned to the semiconductor device 154. Heat is applied to the assembly allowing the solder 160 to flow. Surface tension of the solder 160' after it has become a liquid causes it to remain between the solderable material 150 on the semiconductor device 154 and the solderable material 156 on the transparent lid 158. The solder 160' is identified with a prime (') on the reference numeral to signify that the structure has changed because of flowing and resolidifying. The assembly is heated for a sufficient time to allow the solder 160 to flow and wet all solderable surfaces. Once the heat is removed the solder 160' re-solidifies and the transparent lid 158 is hermetically sealed to the semiconductor device 154 as shown in the cross section view of Figure 4.

Figure 5 shows a cross section view of the lid and the metallization layers. According to the preferred embodiment, the solderable material 156 actually comprises a sandwich of layers. In the preferred embodiment, the solderable layer 156 includes a first layer 156A formed against the transparent lid 158. A second layer 156B is formed over the first layer 156A and the layer of solder 160 is then formed over the second layer 156B. In the preferred embodiment using these layers, the first layer 156A user 300 angstrom layer of chrome and the second layer 156B is a 10,000 angstrom layer of gold. The layer of solder 160 is and 80 Au/ 20 Sn solder 50 microns thick.

According to the preferred embodiment, the transparent lid 158 is segmented prior to forming the metallization layers thereon. The inventors have learned through experimentation that the cost of masking the side edges of the transparent lid 158 exceeds

the cost of the materials. Thus, in actual practice gold and chrome are also formed on the side edges of the transparent lid 158. While this is not preferred, it causes no deleterious effects. As manufacturing processes develop, the golden chrome on the side edges of the transparent lid 158 may be deleted.

Figure 6 shows a cross-section view of another embodiment of the lid and metallization layers. In this embodiment, the solderable material 156 also comprises a sandwich of layers. Here, the solderable layer includes a first layer 156C formed against the transparent lid 158. A second layer 156D is formed over the first layer 156C and a third layer 156E is formed over the second later 156D. the layer of solder 160 is then formed over the third layer 156E. In this embodiment the first layer 156C is a 300 angstrom layer of chrome, the second layer 156D is a him 500 angstrom layer of nickel and the third layer 156E is a 10,000 angstrom layer of gold. The layer of solder 160 is an 80 Au/ 20 Sn solder 50 microns.

Figure 7 shows a cross-section view of an embodiment of the solderable region 152 of the semiconductor device 154. For simplicity, the active portion of the semiconductor device 154 is not shown. The layer of solderable material is actually formed of a sandwich of layers. The sandwich of layers is formed using conventional lift-off semiconductor processing techniques. In other words, a layer of photo resist is deposited onto the surface of the semiconductor wafer. Using conventional masking techniques, openings are formed through the photo resist. The layers of solderable material are then deposited over the wafer including into the openings formed through the photo resist. Upon removal of the photo resist, the solderable material only remains on the surface of the semiconductor wafer in the lid sealing region 152.

A first layer 150A is formed in the lid sealing region 152 of the semiconductor device 154. A second layer 150B is formed over the first layer 150A. In this embodiment, the first layer 150A is a 500 angstrom layer of chrome. The second layer 150B is a 1000 angstrom layer of palladium.

Figure 8 shows they cross-section view of another embodiment of the solderable region 152. In this embodiment, the solderable layer 150 comprises a three layer sandwich. A first layer 150C is formed in the lid sealing region 152 of the semiconductor device 154. A second layer 150D is formed over the first layer 150C and a third layer 150E is formed over the second layer 150D using conventional lift off techniques. In this embodiment, the first layer 150C is a 300 angstrom layer of titanium, the second layer 150D is a 1000 angstrom layer of nickel and the third layer 150E is a 1000 angstrom layer of platinum.

It will be apparent that the angle between the transparent lid 158 and the semiconductor device 154 can affect the optical characteristics of the assembly. For example, optical energy reflecting between the surface of the semiconductor device 154 and the bottom side of the transparent lid 158 can interfere constructively or destructively. There are applications which require the transparent lid 158 and semiconductor device 154 to be parallel and their applications which require a predetermined angle between these elements. The present invention also provides users of this technology and ability to control and select the pre-determined angle between the transparent lid 158 and semiconductor device 154.

Once melted, the solder 160 will flow to all wetted surfaces. However, the surface tension of the solder 160 will prevented from him flowing beyond the boundaries of the

solderable layers 150 and 156. Owing to the viscous properties of solder, the solder and cannot flow circumferentially around the periphery of a ringed structure such as described in this invention.

Because all layers are concurrently formed using conventional semiconductor processing techniques, the thickness of each one of the several layers is uniform throughout each one of the entire layer. To control the relative angle between the transparent lid 158 and semiconductor device 154 the relative width of one side of the solderable layer 150 is adjusted. Figure 9 shows a simplified cross-section of this embodiment. Recall that the lid ceiling region 152 of the semiconductor device 154 is essentially a rectangular ring. The mask for forming the solderable layer 150 is modified along one edge of the rectangular ring to form a wider layer 150'.

Figure 10 shows a cross-section of the embodiment of Figure 9 once the lid 158 has aligned to the semiconductor device 154 and the assembly is heated to hermetically seal the construction. After the solder 168 heated beyond melting point it flows to all wetted surfaces. Because the layer 150' is wider than the layer 150, the solder 160'' must necessarily spread wider than the solder 160'''. Further, because the solder does not flow circumferentially around the periphery of the ringed structure, the transparent lid 158 is closer to the semiconductor device 154 over the wide solderable layer 150' than over the conventional solderable layer 150.

It will be apparent to persons of ordinary skill in the art that the thickness of the resulting solder and hence the angle between the transparent lid 158 and semiconductor device 154 could also be adjusted by modifying the width of the solderable layer 156 which is coupled to the transparent lid 158. The angle could also be adjusted by

concurrently modifying the widths of both the solderable layer 150 and its corresponding solderable layer 156. However, because the wafer of semiconductor devices 154 is made with the sequence of wafer masks, and because the lids are individually aligned to the wafer it is easier to adjust the angle by only adjusting the width of the solderable layer 150 as appropriate.

Figure 11 shows a plan view of a fixture 200 for aligning transparent lids to semiconductor devices on a wafer. Figure 12 shows a side view partially in cross section of the same fixture 200. Common reference numerals will be used to identify identical elements in the Figures 11 and 12. The fixture 200 includes a graphite base 202. The base 202 includes a cut-out 204 appropriately sized to accept a semiconductor wafer. Four threaded locking elements 206 (screws) pass upwardly through the base 202 through a plurality of holes 208.

An intermediate plate 210 includes holes 214 aligned to accept the threaded locking elements 206. The intermediate plate 210 also includes thirty-seven apertures 212 sized to accept the transparent lids 158 (Figure 3). The intermediate plate 210 also includes three channels 216 positioned to allow moisture to escape from the semiconductor devices 154 (Figure 3) during a subsequent heating operation. Alignment pins 218 are mounted to the base 202 and pass through the intermediate plate 210. A pair of holding plates 220 also include holes 222 which are positioned to accept the threaded locking elements 206.

In use, a wafer is aligned and mounted within the cut-out 204 of the base 202 with the semiconductor devices 154 (Figure 3) facing away from the base 202. The intermediate plate 210 is then installed to the base 202 over the wafer. A transparent lid 158 is then inserted into each of the apertures 212. It will be apparent that a test operation

could be performed on the semiconductor devices 154 while still in the wafer form and bad devices could be marked so that no transparent lid 158 need be sealed to such bad devices. A weighted cap-panel 224 is rested over the transparent lids 158 to apply an appropriate amount of downward pressure owing to gravity.

Once the assembly described relative to Figures 11 and 12 is fully constructed it is placed into an environmental chamber. Figure 13 shows a graph representing temperature in °C versus time. Figure 14 shows a graph representing atmospheric pressure in torr and/or atm versus time. Once the ambient atmosphere is removed, the assembly is exposed to a back fill gas comprising 10% He, 10% H and 80% N at less than 1 ppm water. The two graphs of Figures 13 and 14 are displayed in conjunction to a single time line and the process of forming the hermetic seal of the present invention is so described herein.

The assembly is inserted into the environmental chamber with initial conditions of ambient temperature and atmosphere. Immediately, the atmosphere is evacuated to a vacuum pressure of 0.1 torr. This cycle lasts for approximately the first minute. Then the assembly is subjected to a pressure of 2 atm of the back fill gas for about 15 to 30 seconds and then the atmosphere is evacuated to a vacuum pressure of 0.0001 torr. This first evacuation continues and during the evacuation, at about five minutes, the chamber is heated to about 190 °C. This is less than the melting point of the solder. This step of heating is to dry all residual moisture from the semiconductor devices 154 (Figure 3) and also from the lids 158 (Figure 3) and is known as a drying vacuum bake. During the drying vacuum bake, at about 7.5 minutes, the atmosphere is again evacuated to about 0.0001 torr for about one minute. Thereafter, at about 9.5 minutes, the pressure is increased to 2 atm with the back fill gas. Once the pressure reaches 2 atm, at about 10

minutes, the chamber is heated beyond the melting temperature of the solder and held at that temperature for about 3 minutes. The temperature is then allowed to return to room temperature. After the melting temperature is traversed, so that the solder solidifies and the semiconductor device is hermetic, the air pressure is returned to ambient. The heating steps are undertaken by a radiant heat source, though any other convenient means of heating will suffice.

It will be recalled that layers of solderable material must first be formed so that the solder will appropriately adhere to both the lid and the semiconductor device. There are certain advantages to this. With a MEM, it is important that the lid does not interfere with the free movement of the mechanical MEM structure. The layers of solderable material can be used to increase the distance between the lid and the semiconductor device. However, materials other than solder can be used to seal the lids to the semiconductor devices. The materials for the structures can be appropriately substituted as described below.

A polymetric epoxy ring can be formed in the lid sealing region or around the periphery of the lid, or both. The lid and the semiconductor device are then brought together, heated and cooled to passivate the semiconductor device. Depending upon the thickness of the epoxy layer(s) and its relative viscosity, the lid and the semiconductor device may be sufficiently far apart to avoid having the lid interfere with the operation of the MEM. If simple experimental results indicate otherwise, any suitable material can be first deposited in the lid sealing region, around the periphery of the lid, or both to increase the spacing between the lid and the semiconductor device. The spacing material can be SiO_2, for example as that material is readily manufacturable in an conventional

semiconductor manufacturing facility.

Another material that can be used in place of the polymetric epoxy is glass frit. But for this substitution, the glass material can be used in the same way as the polymetric epoxy described above.

It will be apparent to one of ordinary skill in the art that the lids and their respective rings of solderable layers and overlying layers of solder could be formed on a wafer of transparent material. Then the transparent wafer and the semiconductor wafer need merely be fixtured and aligned before subjecting that combination to the temperature cycling taught in Figures 13 and 14. To separate the devices into separate devices, one could simply use a narrow wafer saw blade and cut through the transparent wafer to only a predetermined depth to form individual lids and then in a second operation, use the same narrow blade to separate the semiconductor devices. In an alternate embodiment, a single narrow blade with a berm could be used to separate these devices in a single operation. As shown in Figure 15, the lids 158 are separated by the berm 300 and the semiconductor devices 154 are concurrently separated by the tip of the saw blade 302.

When the lids 158 are all concurrently formed in a wafer and then brought together with a wafer of semiconductor devices 154, it will be apparent to one of ordinary skill in the art that the semiconductor devices 154 and the lids 158 will necessarily be parallel to one another. To form a predetermined angle between the semiconductor devices 154 and the lids 158, either one or both of the semiconductor devices 154 and the lids 158 can have a non-uniform peripheral region as previously described. Once the semiconductor devices 154 and the lids 158 are initially joined together using one of the techniques described above, the assembly is cut to form individual units. Thereafter, these units can be reheated

to allow the seal to flow and provide the desired angle between the semiconductor devices 154 and the lids 158.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A microelectronic machine (MEM) having an hermetic seal comprising:
   a. a substrate on which is formed an active MEM device;
   b. a lid sealing region surrounding the active MEM device;
   c. a first layer of solderable material formed over the lid sealing region;
   d. a layer of solder formed over the first layer of solderable material;
   e. a second layer of solderable material formed over the solder; and
   f. a lid formed over the second layer of solderable material forming an hermetic seal thereby.

2. The MEM according to claim 1 wherein the first layer of solderable material is a sandwich comprising chrome adjacent the lid sealing region and paladium adjacent the solder.

3. The MEM according to claim 1 wherein the first layer of solderable material is a sandwich comprising titanium adjacent the lid sealing region, nickel adjacent the titanium and platinum between the nickel and the solder.

4. The MEM according to claim 1 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder and chrome adjacent the lid.

5. The MEM according to claim 1 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder, nickel adjacent the gold and chrome between the nickel and the lid.

6. A display device comprising:

a. a light modulator formed on a semiconductor substrate;

b. a lid sealing region surrounding the light modulator;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the light modulator;

d. a first layer of solderable material formed over the lid sealing region;

e. a layer of solder formed over the first layer of solderable material;

f. a second layer of solderable material formed over the solder; and

g. a transparent lid formed over the second layer of solderable material forming an hermetic seal thereby.

7. The display device according to claim 6 wherein the light modulator is a diffraction grating light valve.

8. The display device according to claim 6 wherein the first layer of solderable material is a sandwich comprising chrome adjacent the lid sealing region and paladium adjacent the solder.

9. The display device according to claim 6 wherein the first layer of solderable

material is a sandwich comprising titanium adjacent the lid sealing region, nickel adjacent the titanium and platinum between the nickel and the solder.

10. The display device according to claim 6 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder and chrome adjacent the lid.

11. The display device according to claim 6 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder, nickel adjacent the gold and chrome between the nickel and the lid.

12. A method of forming an hermetic seal to a semiconductor device comprising the steps of:

a. forming an active semiconductor device on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding the active semiconductor device;

c. forming means for electrically coupling to the active semiconductor device on the surface of the substrate and outside the lid sealing region;

d. forming a first layer of solderable material on the lid sealing region;

e. on an optically transparent lid, forming a second layer of solderable material in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the lid to the lid sealing region.

13. A method of forming an hermetic seal between a lid and a semiconductor device, wherein the lid and the semiconductor device are parallel to one another comprising the steps of:

a. providing an active semiconductor device on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding the active semiconductor device;

c. forming means for electrically coupling to the active semiconductor device on the surface of the substrate and outside the lid sealing region;

d. forming a first layer of solderable material on the lid sealing region;

e. on an optically transparent lid, forming a second layer of solderable material in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the lid to the lid sealing region,

wherein the first layer of solderable material and the second layer of solderable material each have a substantially uniform cross section around their respective lengths.

14. A method of forming an hermetic seal between a lid and a semiconductor device, wherein the lid and the semiconductor device are not parallel to one another comprising the steps of:

a. providing an active semiconductor device on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding the active semiconductor device;

c. forming means for electrically coupling to the active semiconductor device on the surface of the substrate and outside the lid sealing region;

d. forming a first layer of solderable material on the lid sealing region;

e. on an optically transparent lid, forming a second layer of solderable material in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the lid to the lid sealing region,

wherein at least one of the first layer of solderable material and the second layer of solderable material each have a substantially non-uniform cross section around their respective lengths.

15. The method according to claim 14 wherein the lid sealing region and the first layer of solderable material have a substantially rectangular configuration having four legs joined at substantially right angles and one of the legs of the first layer of solderable material has a substantially dissimilar cross sectional area from the other three legs.

16. A method of concurrently forming an hermetic seal to each of a plurality of semiconductor devices all formed on a single semiconductor wafer comprising the steps of:

a. providing a plurality of active semiconductor devices on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding each of the active semiconductor devices;

c. forming means for electrically coupling to each of the active semiconductor devices on the surface of the substrate and outside the lid sealing region for each of the active semiconductor devices;

d. forming a first layer of solderable material on each of the lid sealing regions;

e. on an optically transparent wafer, forming a second layer of solderable material in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the wafer to the lid sealing regions.

17. A method of forming an hermetic seal between a transparent wafer and a semiconductor wafer having a plurality of semiconductor devices, wherein the transparent wafer and the semiconductor wafer are parallel to one another comprising the steps of:

a. providing a wafer having a plurality of active semiconductor devices on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding each one of the active semiconductor devices;

c. forming means for electrically coupling to each one of the active semiconductor devices on the surface of the substrate and outside each one of the lid sealing regions;

d. forming a first layer of solderable material on each one of the lid sealing regions;

e. on an optically transparent wafer, forming a second layer of solderable material

in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the optically transparent wafer to the lid sealing regions,

wherein the first layer of solderable material and the second layer of solderable material each have a substantially uniform cross section around their respective lengths.

18. A method of forming an hermetic seal between a plurality of lids from an optically transparent wafer and a wafer of semiconductor devices, wherein at least one of the lids and its respective semiconductor device are not parallel to one another, the method comprising the steps of:

a. providing a plurality of active semiconductor devices on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding each one of the active semiconductor devices;

c. forming means for electrically coupling to each one of the active semiconductor devices on the surface of the substrate and outside each respective one of the lid sealing regions;

d. concurrently forming a first layer of solderable material on the lid sealing regions;

e. on an optically transparent wafer, forming a second layer of solderable material in a pattern conforming to the first layer of solderable material;

f. aligning the first layer of solderable material to the second layer of solderable material while providing a layer of solder therebetween; and

g. applying heat to melt the solder and seal the wafer to the lid sealing regions,

wherein at least one of the first layer of solderable material and the second layer of solderable material each have a substantially non-uniform cross section around their respective lengths;

h. concurrently separating the semiconductor devices from the lids to form units; and

i. re-heating the units to provide a non-parallel relationship between the lids and their respective semiconductor devices.

19. The method according to claim 18 wherein the lid sealing region and the first layer of solderable material have a substantially rectangular configuration having four legs joined at substantially right angles and one of the legs of the first layer of solderable material has a substantially dissimilar cross sectional area from the other three legs.

20. A microelectronic machine (MEM) having an hermetic seal comprising:

a. a substrate on which is formed an active MEM device;

b. a lid sealing region surrounding the active MEM device;

c. a layer polymetric epoxy formed over the lid sealing region; and

d. a lid formed over the layer of polymetric epoxy forming an hermetic seal thereby.

21. The MEM according to claim 20 further comprising a spacing layer formed between the layer of polymetric epoxy and the active MEM device.

22. The MEM according to claim 20 further comprising a spacing layer formed between the layer of polymetric epoxy and the lid.

23. A display device comprising:

a. a light modulator formed on a semiconductor substrate;

b. a lid sealing region surrounding the light modulator;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the light modulator;

d. a layer of polymetric epoxy formed over the lid sealing region; and

e. a transparent lid formed over the layer of polymetric epoxy forming an hermetic seal thereby.

24. The display device according to claim 23 wherein the light modulator is a diffraction grating light valve.

25. The display device according to claim 23 further comprising a spacing layer formed between the layer of polymetric epoxy and the display device.

26. The display device according to claim 23 further comprising a spacing layer formed between the layer of polymetric epoxy and the lid.

27. A method of forming an hermetic seal to a semiconductor device comprising the steps of:

a. providing an active semiconductor device on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding the active semiconductor device;

c. forming means for electrically coupling to the active semiconductor device on the surface of the substrate and outside the lid sealing region;

d. forming a layer of polymetric epoxy on the lid sealing region;

e. providing an optically transparent lid sized to conform to the lid sealing region;

f. aligning the lid to the layer of polymetric epoxy; and

g. applying heat to melt the polymetric epoxy and seal the lid to the lid sealing region.

28. The method according to claim 27 further comprising a spacing layer formed between the layer of polymetric epoxy and the display device.

29. The method according to claim 27 further comprising a spacing layer formed between the layer of polymetric epoxy and the lid.

30. A microelectronic machine (MEM) having an hermetic seal comprising:

a. a substrate on which is formed an active MEM device;

b. a lid sealing region surrounding the active MEM device;

c. a layer glass frit formed over the lid sealing region; and

d. a lid formed over the layer of glass frit forming an hermetic seal thereby.

31. The MEM according to claim 30 further comprising a spacing layer formed between the layer of glass frit and the active MEM device.

32. The MEM according to claim 30 further comprising a spacing layer formed between the layer of glass frit and the lid.

33. A display device comprising:

a. a light modulator formed on a semiconductor substrate;

b. a lid sealing region surrounding the light modulator;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the light modulator;

d. a layer of glass frit formed over the lid sealing region; and

e. a transparent lid formed over the layer of glass frit forming an hermetic seal thereby.

34. The display device according to claim 33 wherein the light modulator is a diffraction grating light valve.

35. The display device according to claim 33 further comprising a spacing layer formed between the layer of glass frit and the display device.

36. The display device according to claim 33 further comprising a spacing layer formed between the layer of glass frit and the lid.

37. A method of forming an hermetic seal to a semiconductor device comprising the steps of:

a. providing an active semiconductor device on a semiconductor substrate;

b. forming a substantially planarized lid sealing region surrounding the active semiconductor device;

c. forming means for electrically coupling to the active semiconductor device on the surface of the substrate and outside the lid sealing region;

d. forming a layer of glass frit on the lid sealing region;

e. providing an optically transparent lid sized to conform to the lid sealing region;

f. aligning the lid to the layer of glass frit; and

g. applying heat to melt the glass frit and seal the lid to the lid sealing region.

38. The method according to claim 37 further comprising a spacing layer formed between the layer of glass frit and the display device.

39. The method according to claim 37 further comprising a spacing layer formed between the layer of glass frit and the lid.

40. An optical device comprising:

a. a MEM formed on a semiconductor substrate;

b. a lid sealing region surrounding the MEM;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the MEM;

d. a first layer of solderable material formed over the lid sealing region;

e. a layer of solder formed over the first layer of solderable material;

f. a second layer of solderable material formed over the solder; and

g. a transparent lid formed over the second layer of solderable material forming an hermetic seal thereby.

41. The optical device according to claim 40 wherein the first layer of solderable material is a sandwich comprising chrome adjacent the lid sealing region and paladium adjacent the solder.

42. The optical device according to claim 40 wherein the first layer of solderable material is a sandwich comprising titanium adjacent the lid sealing region, nickel adjacent the titanium and platinum between the nickel and the solder.

43. The optical device according to claim 40 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder and chrome adjacent the lid.

44. The optical device according to claim 40 wherein the second layer of solderable material is a sandwich comprising gold adjacent the solder, nickel adjacent the gold and

chrome between the nickel and the lid.

45. An optical device comprising:

a. a MEM formed on a semiconductor substrate;

b. a lid sealing region surrounding the MEM;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the MEM;

d. a layer of polymetric epoxy formed over the lid sealing region; and

e. a transparent lid formed over the layer of polymetric epoxy forming an hermetic seal thereby.

46. The optical device according to claim 45 further comprising a spacing layer formed between the layer of polymetric epoxy and the MEM.

47. The optical device according to claim 45 further comprising a spacing layer formed between the layer of polymetric epoxy and the lid.

48. An optical device comprising:

a. a MEM formed on a semiconductor substrate;

b. a lid sealing region surrounding the MEM;

c. a plurality of bond pads positioned adjacent the lid sealing region and away from the MEM;

d. a layer of glass frit formed over the lid sealing region; and

e. a transparent lid formed over the layer of glass frit forming an hermetic seal thereby.

49. The optical device according to claim 48 further comprising a spacing layer formed between the layer of glass frit and the MEM.

50. The optical device according to claim 48 further comprising a spacing layer formed between the layer of glass frit and the lid.

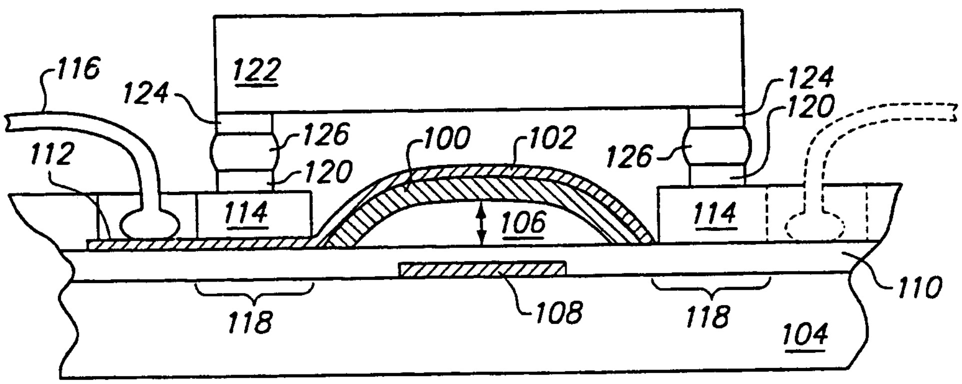
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FIG. 1

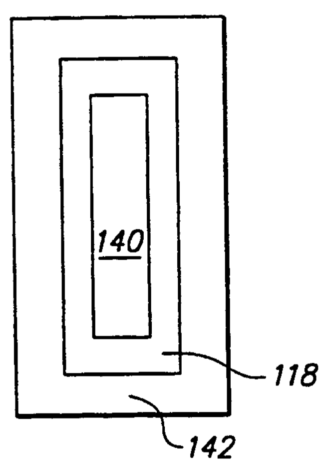
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FIG. 2

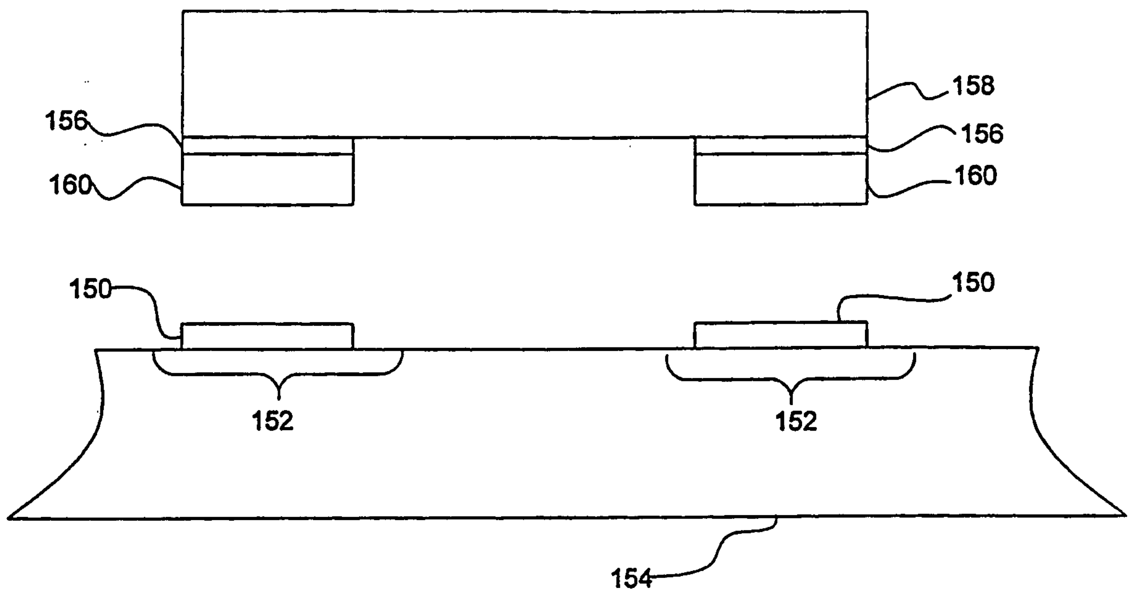

FIGURE 3

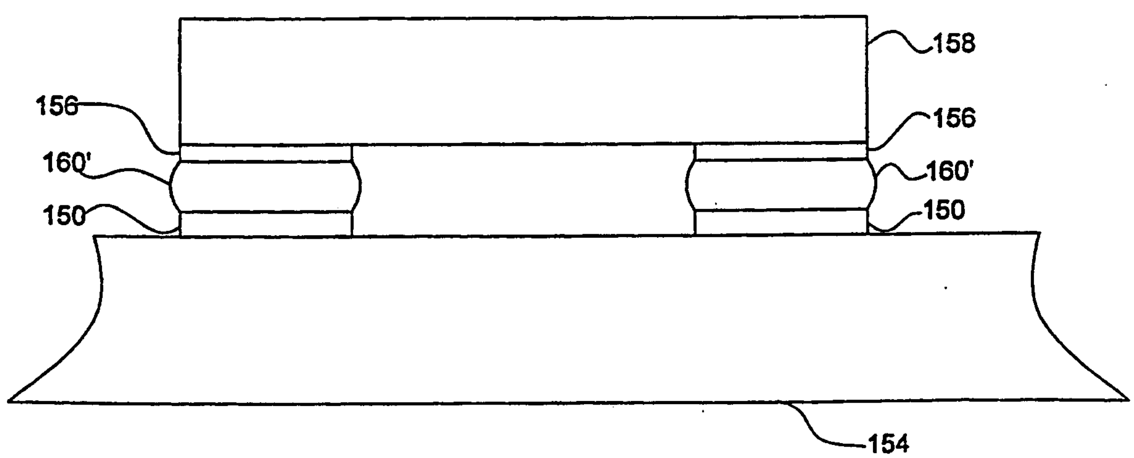

FIGURE 4

FIGURE 5

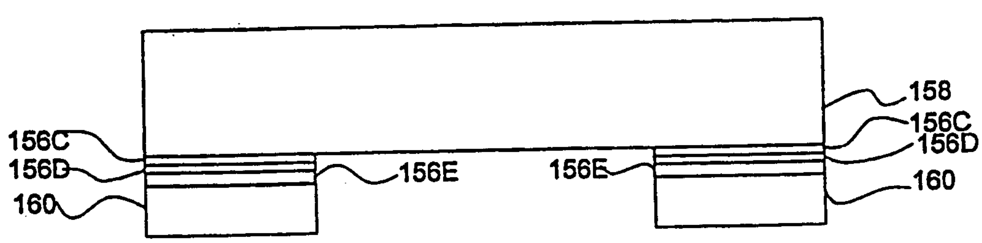

FIGURE 6

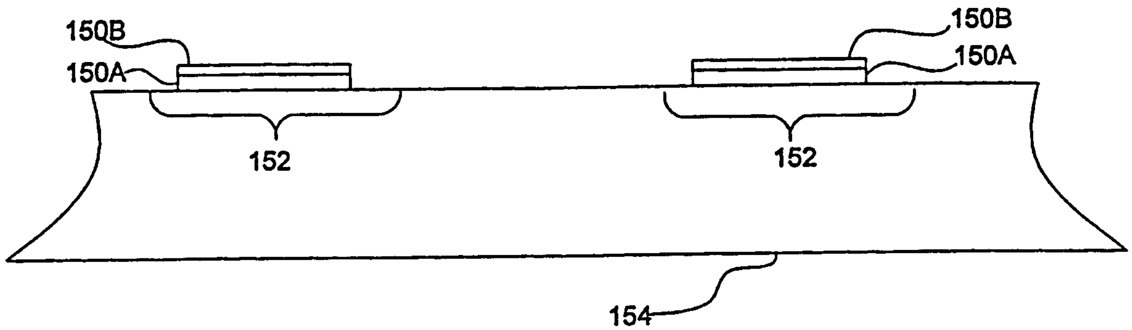

FIGURE 7

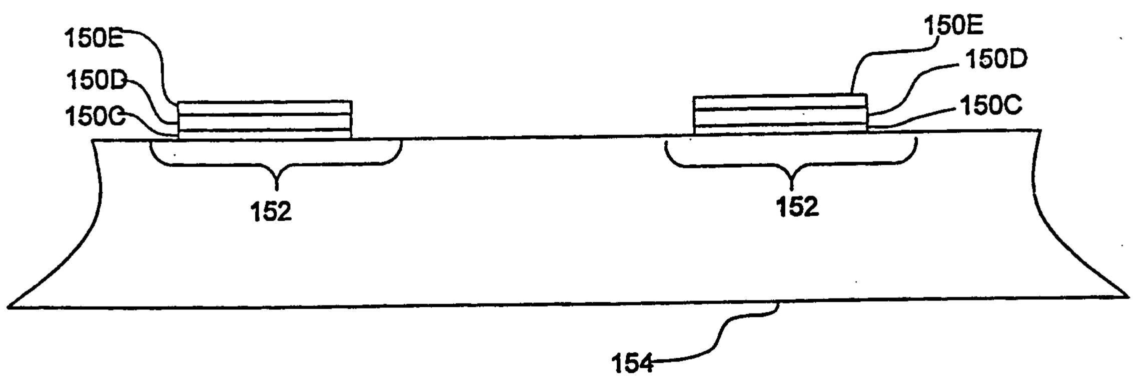

FIGURE 8

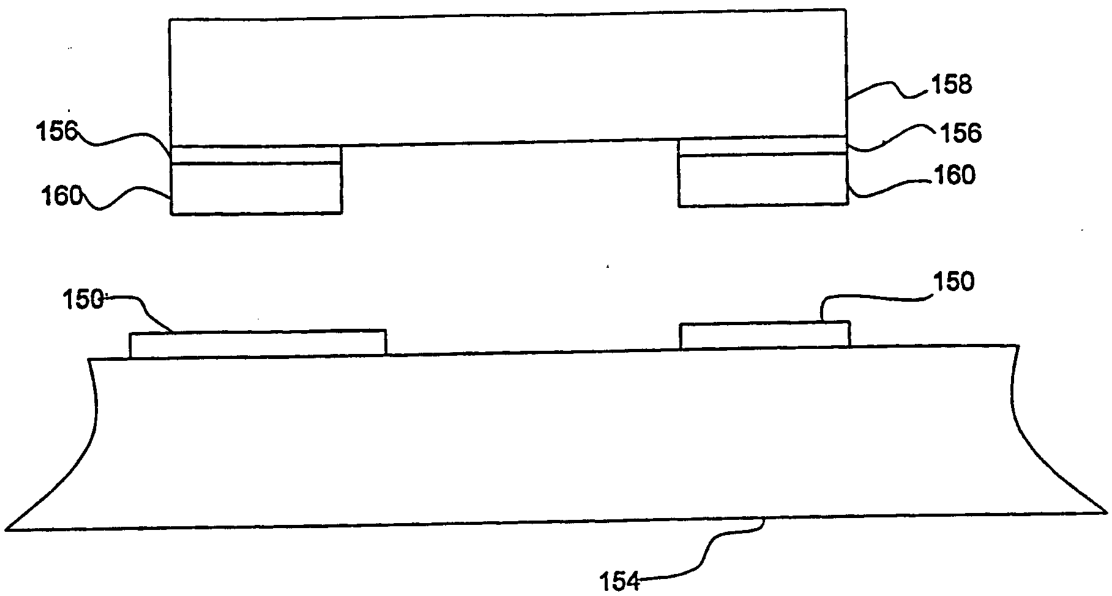

FIGURE 9

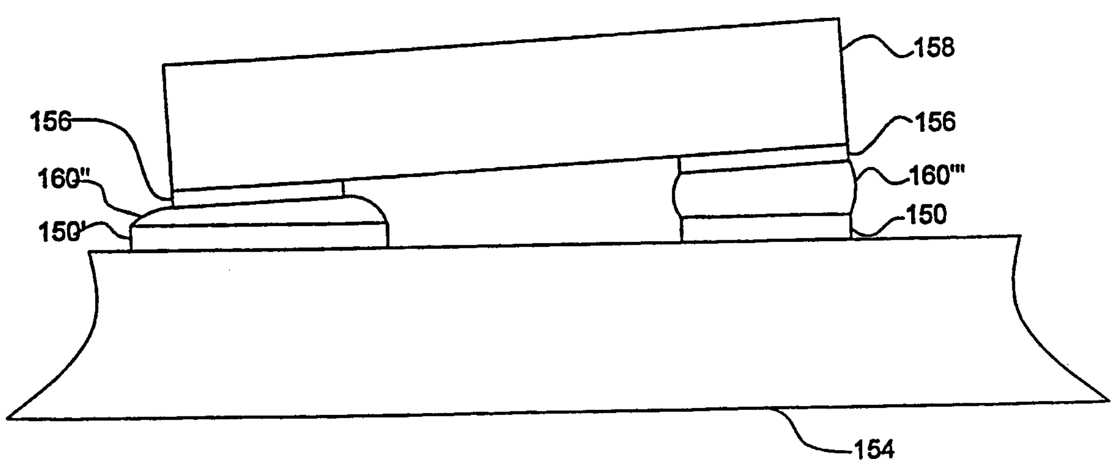

FIGURE 10

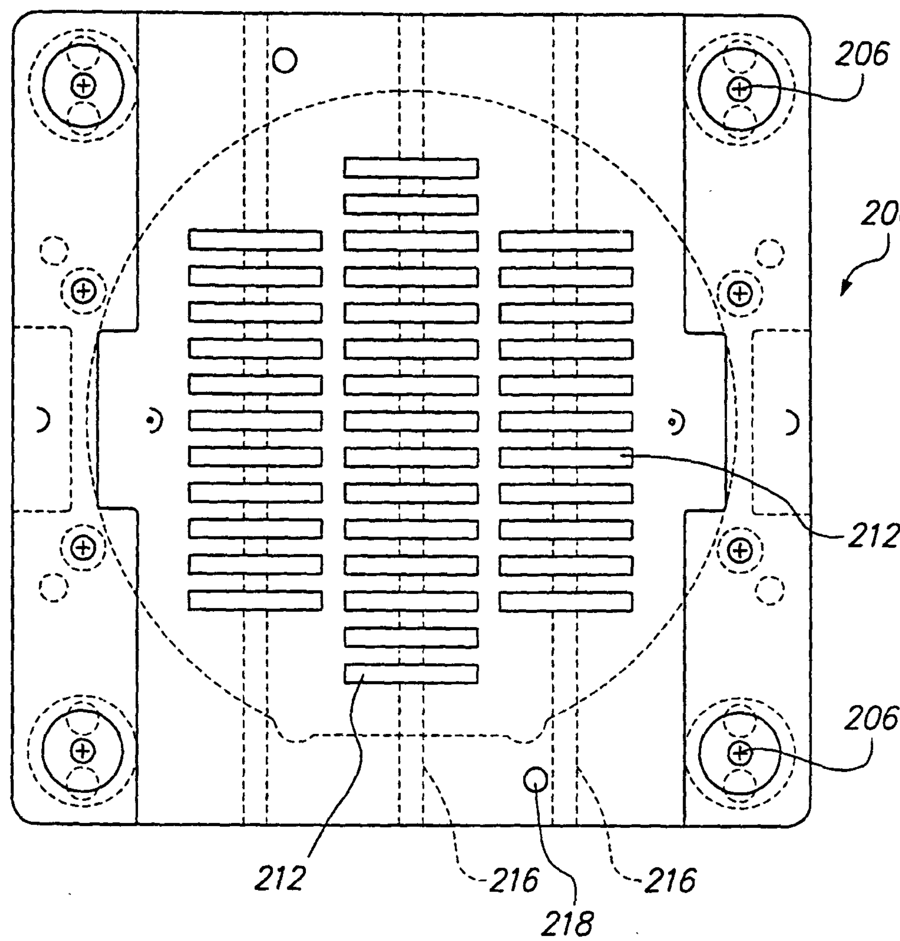
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FIG. 11

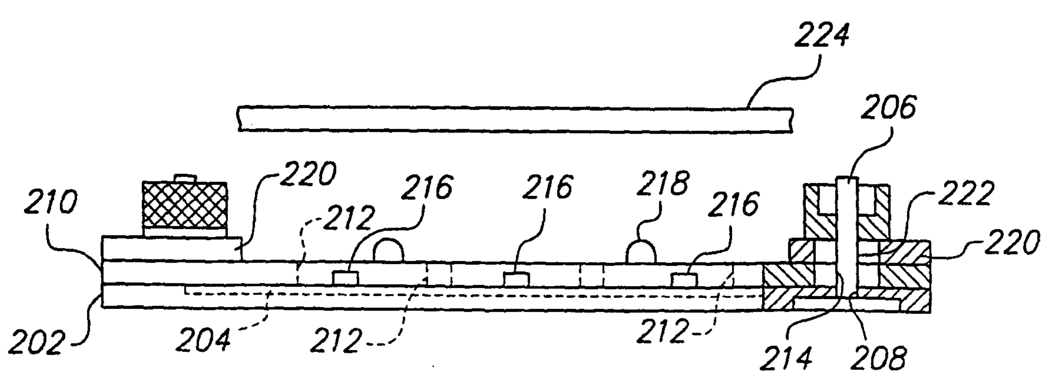
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FIG. 12

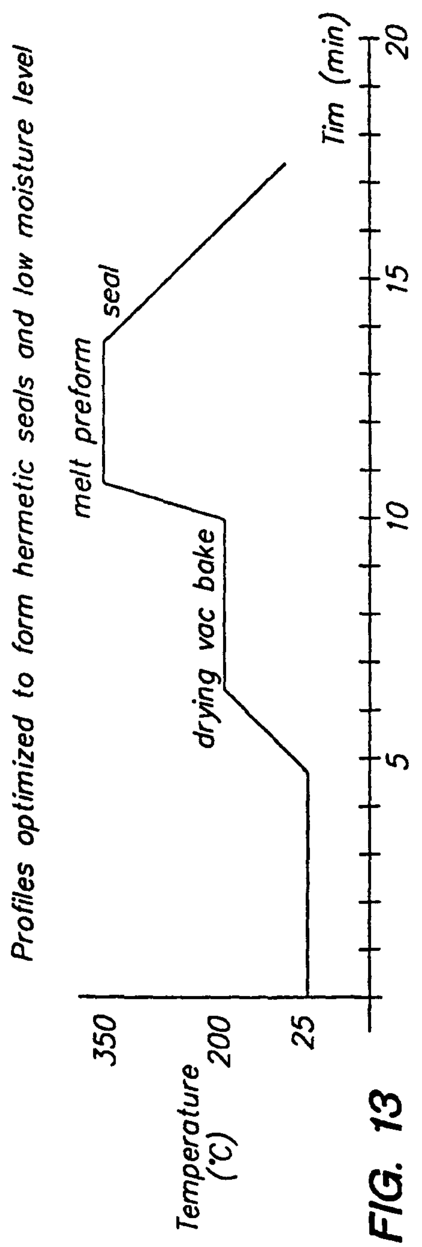
Profiles optimized to form hermetic seals and low moisture level
Temperature (°C)
350
200
25
melt preform
seal
drying vac bake
5
10
15
20
Tim (min)

FIG. 13

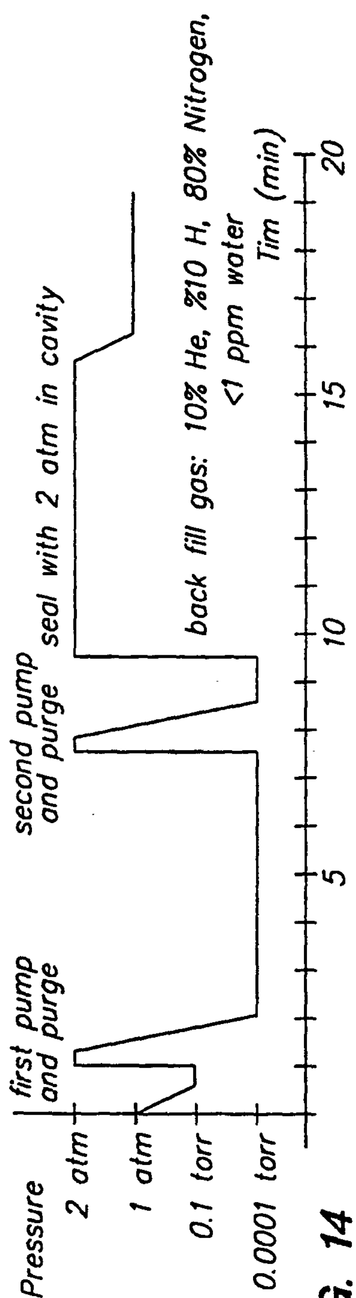
Pressure
2 atm
1 atm
0.1 torr
0.0001 torr
first pump and purge
second pump and purge
seal with 2 atm in cavity
back fill gas: 10% He, %10 H, 80% Nitrogen, <1 ppm water
5
10
15
20
Tim (min)

FIG. 14

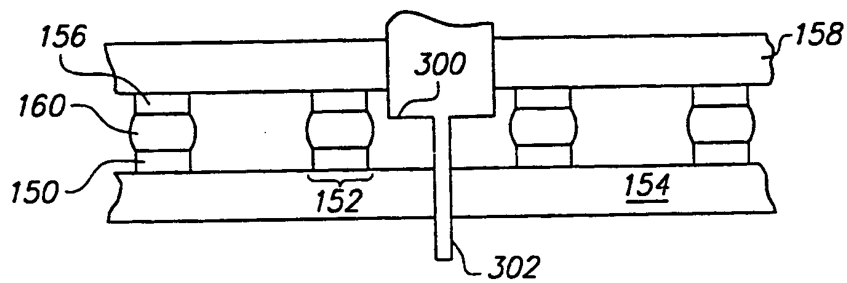

FIG. 15

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(72) Inventor: SHOOK, James, Gill; 179 Montclair Drive, Santa Cruz, CA 95960 (US).

(74) Agents: HAVERSTOCK, Thomas, B. et al.; Haverstock & Owens LLP, Suite 420, 260 Sheridan Avenue, Palo Alto, CA 94306 (US).

(81) Designated States: AL, AM, AU, BB, BG, BR, CA, CN, CZ, EE, ES, FI, GE, HU, IS, JP, KG, KP, KR, LK, LR, LT, LV, MD, MG, MK, MN, MX, NO, NZ, PL, RO, SG, SI, SK, TR, TT, UA, UZ, VN, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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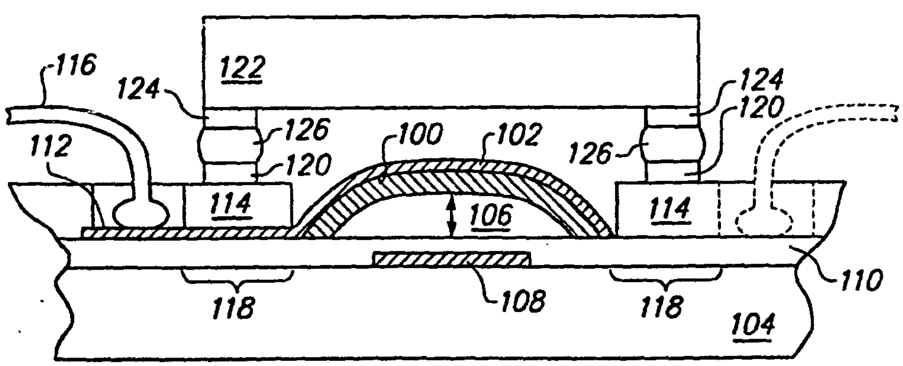
(54) Title: METHOD OF AND APPARATUS FOR SEALING AN HERMETIC LID TO A MICROELECTRONIC MACHINE



(57) Abstract

A method and apparatus of hermetically passivating a semiconductor device includes sealing a lid directly onto a semiconductor substrate. An active device is formed on the surface of the substrate and is surrounded by a substantially planar lid sealing region, which in turn is surrounded by bonding pads. A first layer of solderable material is formed on the lid sealing region. A lid is provided which has a second layer of solderable material in a configuration corresponding to the first layer. A solder is provided between the first layer and second layer of solderable materials. In the preferred embodiment, the solder is formed over the second layer. Heat is provided to hermetically join the lid to the semiconductor device without requiring a conventional package. Preferably the first and second layers are sandwiches of conventionally known solderable materials which can be processed using conventional semiconductor techniques. An angle between the lid and the semiconductor device can be controlled by adjusting relative widths of one or both the layers of solderable materials.

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INTERNATIONAL SEARCH REPORT

Inte. onal Application No
PCT/US 99/17131

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81B7/00 H01L23/10 G02B5/18 G02B26/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	EP 0 851 492 A (TEXAS INSTRUMENTS INC) 1 July 1998 (1998-07-01)	1,6, 12-14, 16-18, 20,21, 23,25, 27,28, 30,31, 33,35, 37,38, 40,45, 46,48,49
Y	abstract page 4, column 5, line 47 - line 55; figure 2 ---	4,10,43
Y	US 3 657 610 A (SHIRAISHI MASAMICHI ET AL) 18 April 1972 (1972-04-18) column 2, line 52 - line 65 ---	4,10,43
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 January 2000	27.01.00

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PCT/US 99/17131

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 744 752 A (MCHERRON DALE C ET AL) 28 April 1998 (1998-04-28) column 4, line 19 -column 5, line 14 ---	5,11,44
A	WO 90 13913 A (EASTMAN KODAK CO) 15 November 1990 (1990-11-15) page 3, line 15 -page 4, line 13 page 5, line 8 - line 27 ---	1-19, 40-44
A	WO 98 05935 A (INTEGRATED SENSING SYSTEMS INC) 12 February 1998 (1998-02-12) the whole document ---	1-50
A	DE 43 23 799 A (TOSHIBA KAWASAKI KK) 20 January 1994 (1994-01-20) column 16, line 41 - line 61 ---	2-5, 8-11,41, 42
A	WO 96 02941 A (JOHNSON MATTHEY ELECT INC) 1 February 1996 (1996-02-01) the whole document ---	2-5, 8-11,41, 42
A	EP 0 089 044 A (NIPPON ELECTRIC CO) 21 September 1983 (1983-09-21) abstract; figures -----	21,22, 25,26, 28-39, 46-50

INTERNATIONAL SEARCH REPORT	I. ..national application No. PCT/US 99/17131

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see additional sheet

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☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-19, 40-44

   A hermetic lid for a MEMC seald by soldering

2. Claims: 20-29, 45-47

   A hermetic lid for a MEMC seald by polymetric epoxy

3. Claims: 30-39, 48-50

   A hermetic lid for a MEMC seald by a glass frit

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/US 99/17131

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